

IN THE CLAIMS:

Please amend the following claims.

CLEAN VERSION OF AMENDED CLAIMS:

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1 1. (Amended) A method of forming a transistor, comprising:  
2 forming an alignment component on a substrate of a semiconductor  
3 material;  
4 depositing a metal layer over the substrate and the alignment component;  
5 reacting the metal layer with the semiconductor material of the substrate to  
6 form two silicide regions, the silicide regions having inner surfaces which face  
7 one another, wherein an upper portion of each inner surface contacts the  
8 alignment component and a lower portion of each inner surface contacts the  
9 semiconductor material of the substrate; and  
10 replacing the alignment component with a conductive gate.

1 2. The method of claim 1 wherein the alignment component is non-  
2 conductive.

1 3. The method of claim 2 wherein the alignment component is made of a  
2 material selected from the group consisting of a silicon oxide and silicon nitride.

1 4. The method of claim 1 wherein the alignment component is made of a  
2 material which does not react with the metal layer when the metal layer is  
3 reacted with the semiconductor material of the substrate.

1 5. The method of claim 1 wherein the alignment component has a thickness of  
2 between 1000Å and 2500Å.

1 6. The method of claim 1 wherein the alignment component is less than 0.10  
2 microns wide.

1 7. The method of claim 1 wherein the metal layer is selected from the group  
2 consisting of a material comprising tungsten, cobalt and titanium.

1 8. The method of claim 1 wherein the metal layer is between 300Å and 400 Å  
2 thick.

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1 9. (Amended) The method of claim 1 wherein the silicide regions have lower  
2 surfaces located lower than a lower surface of the alignment component.

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1 10. (Amended) The method of claim 1 wherein the alignment component is  
2 replaced with the gate according to a method comprising:  
3 depositing a layer over the silicide regions and the alignment component;  
4 planarizing the layer at least until the alignment component is exposed;  
5 etching the alignment component at least until the substrate is exposed to  
6 leave an opening between the inner surfaces of the silicide regions; and  
7 forming the gate in the opening.

1 11. (Amended) The method of claim 10 wherein, after the etching of the  
2 alignment component, the upper portions of the inner surfaces are exposed.

1 12. The method of claim 10 wherein the alignment component and the layer  
2 are made of different materials, one being made of a silicon oxide and the other  
3 being made of silicon nitride.

1 13. The method of claim 1 wherein the gate is formed according to a method  
2 comprising:  
3 depositing a gate dielectric layer; and  
4 forming a gate electrode on the gate dielectric layer.

1 14. The method of claim 13 wherein the gate dielectric layer is less than 10Å  
2 thick.

1 15. The method of claim 13 wherein the gate electrode is made out of a metal.

1 16. The method of claim 1, further comprising:  
2 forming doped regions which extend from the silicide regions in  
3 underneath the gate.

1 17. The method of claim 13 wherein the gate dielectric layer has a dielectric  
2 constant of at least 100.

1 18. The method of claim 13 wherein the gate dielectric layer comprises a  
2 material selected from the group consisting of strontium titanate, and barium  
3 strontium titanate.